CLAIMS

What is claimed is:

1. A process for fabricating an electronic component, comprising:

establishing a suitable plating mask for the desired electronic component, on a first surface of a metal carrier;

depositing a plurality of metallic layers on exposed portions of said first surface of said metal carrier; and

stripping said plating mask from said metal carrier to thereby leave said plurality of metallic layers in the form of said electronic component.

2. The process according to claim 1, wherein said establishing a suitable plating mask comprises:

depositing a photo-imageable mask on the first surface of the metal carrier;

imaging said mask to provide imaged portions that define the desired electronic component; and

developing said mask to remove the imaged portions of the mask.

3. The process according to claim 2, wherein said establishing a suitable plating mask comprises establishing a suitable plating mask for at least one capacitor, at least one inductor or a capacitor and an inductor.

4. The process according to claim 1, wherein said electronic component is a capacitor and said process further comprises depositing a dielectric material between plates of said capacitor.

5. A process for fabricating an integrated circuit package, comprising:

establishing a plating mask on a first surface of a metal carrier, the plating mask defining a plurality of components including at least one die attach pad, at least one row of contact pads and at least one additional electronic component;

depositing a plurality of metallic layers on exposed portions of said first surface of said metal carrier, thereby forming said plurality of components;

stripping said plating mask from said metal carrier and leaving said plurality of

metallic layers in the form of said plurality of components;

mounting at least one semiconductor die to a respective one of said at least one die attach pad such that each die attach pad has a respective semiconductor die mounted thereon and pads of each said respective semiconductor die are electrically connected to ones of said contact pads and to said at least one additional electronic component;

overmolding said first surface of said metal carrier to encapsulate said plurality of components and said at least one semiconductor die; and

etching away said metal carrier.

6. The process according to claim 5, wherein etching away said metal carrier includes etching a first one of said metallic layers, thereby providing indentations at each of said plurality of components.

7. The process according to claim 6, further comprising solder mask printing to cover passive ones of said components and leaving exposed portions of said components in ones of said indentations.

8. The process according to claim 7, wherein said solder mask printing forms a pattern for solder ball attachment to said at least one die attach pad and said contact pads and said process further comprises fixing a plurality of solder balls at said exposed portions of said components.

9. The process according to claim 5, wherein said at least one additional electronic component is selected from the group consisting of at least one capacitor, at least one inductor and both a capacitor and an inductor.

10. The process according to claim 5, wherein said establishing a plating mask comprises establishing a plating mask on a first surface of a metal carrier, the plating mask defining a plurality of components including two die attach pads, at least one row of contact pads, an inductor and a capacitor.

11. The process according to claim 10, wherein said inductor and said capacitor are disposed between said die attach pads.

12. The process according to claim 5, wherein said mounting at least one semiconductor die comprises:

mounting each said at least one semiconductor die to said respective one of said at least one die attach pad; and

wire bonding each said at least one semiconductor die to ones of said contact pads and to said additional electronic component.

13. The process according to claim 5, wherein in said establishing a plating mask on said first surface of a metal carrier, said plurality of components further includes a circuit pattern of traces extending from said at least one row of contact pads to ends proximal said die attach pad.

14. The process according to claim 13, wherein in said establishing a plating mask on said first surface of a metal carrier, said additional electronic component comprises at least one capacitor and said circuit pattern further includes a respective trace extending in from each said at least one capacitor, to an end proximal said die attach pad.

15. The process according to claim 14, wherein said mounting at least one semiconductor die comprises:

mounting each said at least one semiconductor die to said respective one of said at least one die attach pad; and

wire bonding each said semiconductor die to ones of the traces.

16. The process according to claim 14, wherein said mounting at least one semiconductor die comprises:

mounting each said at least one semiconductor die in a flip chip orientation to said respective one of said at least one die attach pad such that pads of said semiconductor die are electrically connected to ones of said traces.

17. The process according to claim 5, further comprising singulating to isolate said integrated circuit package from other packages.

18. The process according to claim 5, wherein depositing a plurality of metallic layers on exposed portions of said first surface of said metal carrier, includes further masking between depositing of said metallic layers to thereby selectively plate.

19. The process according to claim 5, wherein said establishing a plating mask comprises:

depositing a photo-imageable mask on the first surface of the metal carrier;

imaging said mask to provide imaged portions that define the desired electronic component; and

developing said mask to remove the imaged portions of the mask.

20. An integrated circuit package comprising:

a plurality of components including at least one die attach pad, at least one row of contact pads and at least one additional electronic component, said plurality of components comprising a plurality of metallic layers;

at least one semiconductor die mounted to a respective one of said at least one die attach pad and electrically connected to said ones of said contact pads and to said at least one additional electronic component;

an overmold covering said at least one semiconductor die and said plurality of components.

21. The integrated circuit package according to claim 20, wherein said plurality of components are indented from said overmold covering.

22. The integrated circuit package according to claim 20, further comprising a solder mask covering passive ones of said components.

23. The integrated circuit package according to claim 22, further comprising a plurality of solder balls fixed to active ones of said components.

24. The integrated circuit package according to claim 20, wherein said plurality of components comprises two die attach pads, at least one row of contact pads, an inductor and a capacitor.

25. The integrated circuit package according to claim 22, wherein said inductor and said capacitor are disposed between said die attach pads and each semiconductor die is electrically connected to said inductor and said capacitor.

26. The integrated circuit package according to claim 20, wherein each of said at least one semiconductor die is mounted to the respective one of the at least one die attach pad and wire bonds connect pads of each of said at least one semiconductor die with ones of said contact pads and with said at least one additional electronic component.

27. The integrated circuit package according to claim 20, wherein said components further include a circuit pattern of a plurality of traces extending from said at least one row of contact pads to ends proximal said at least one die attach pad.

28. The integrated circuit package according to claim 27, wherein said additional electronic component comprises at least one capacitor and one of said plurality of traces includes a respective trace extending in from each said at least one capacitor.

29. The integrated circuit package according to claim 28, wherein each of said at least one semiconductor die is mounted to said respective one of said at least one die attach pad and wire bonds connect each said at least one semiconductor die to ones of the traces.

30. The integrated circuit package according to claim 28, wherein at least one of said at least one semiconductor die is flip chip mounted to said respective one of said at least one die attach pad such that pads of said semiconductor die are electrically connected to ones of said traces.